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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/541,857 | 04/03/2000 | James Digby Collier | 491.039US1 | 4161 |

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| EXAMINER | |
|---|---|
| LAM, TUAN THIEU | |
| ART UNIT | PAPER NUMBER |
| 2816 | |

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application N . | Applicant(s) | |
|---|---|---|---|
| | 09/541,857 | COLLIER ET AL. | |
| | Examin r | Art Unit | |
| | Tuan T. Lam | 2816 | |

*-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *59-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

This is a response to the amendment filed 8/22/2002. The pending claims are 59-84.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 73-74 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 73, the recitation of "each latch circuit comprises two pairs of n-channel transistors operable to control the state of said memory arrangement" is unclear as to which figure should claim 73 reads on. Applicant is required to particularly point out the two pair of n-channel transistors.

Claim 74 is indefinite because of the technical deficiencies of claim 73.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 59-70, 72-82 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USP 4,356,411), prior art of record. Figure 5 of Suzuki et al. shows a frequency divider circuit (267) comprising a first signal means (not shown) to generate a first periodic signal (CLOCK) to be frequency divided by the frequency divider (267), said frequency

divider comprises an input terminal for receiving the first periodic signal, an even number of amplifier stages (two amplifier stages 241, 242) connected in series, with an output of a last amplifier stage (242) connected to input of a first amplifier stage (241) and each amplifier each having an associated propagation delay and a transistor (254, 256, 269, 271) coupled between a supply terminal Vdd and a reference terminal ground for modulating delay through the associated amplifier, wherein the first periodic signal (CLOCK) applied to the first input terminal to a control electrode of the transistor 254, 256 of the odd amplifier stage (241), an even amplifier (242) is activated in anti-phase of the first periodic signal (CLOCK/), the propagation delay through the associated odd and even amplifier stages (241, 242) about half the period of the first periodic signal so that when the propagation delay through the even amplifier stage (242) decreases, the propagation delay through the odd amplifier stage increases, and an output terminal (Q, Q/) for outputting a generated frequency divided signal.

The differences seen between Suzuki et al. and the present invention are: (1) Suzuki et al. uses a single periodic signal (CLOCK) for both even and odd amplifiers instead of the periodic signal and its complementary for even and odd amplifiers stage, respectively, (2) Suzuki et al.'s periodic signal is a square wave instead of an analogue periodic signal as called for in claims 59, 75 and 84. Although Suzuki et al. uses a single clock, one skilled in the art would have recognize that the even and odd amplifiers (241 and 242) are responsive to positive edges and negative edges, respectively. That is, the even and odd amplifiers (241, 242) operate on complementary phases of the clock signal. One skilled in the art would have been recognized that the P-channel transistors 269, 271 receiving the CLOCK signal is functionally equivalent to N channel transistors receiving the opposite phase of the clock signal (CLOCK). Therefore, it

would have been obvious to person skilled in the art at the time of the invention was made to replace the P channel transistors 269, 271 coupled to the clock signal (CLOCK) with N channel transistors coupled to an inverter for receiving a complementary of the clock signal because the substitution is equivalent and will not alter the operation of the frequency divider.

Regarding the input signals being analog periodic signals over square wave signals, one skilled in the art would have recognized that Suzuki et al. would perform substantially the same frequency dividing function for both square wave and analog signals. Since, the field effect transistors are voltage control device, with the analog signal, the field effect transistors will be fully opened or fully closed but to act as variable resistances (see Schilling et al., pages 141 and 147-149). Therefore, outside of non-obvious results, the obvious of using analog signals as input signals instead of square wave to vary the resistance of field effect transistors in a frequency divider will not be patentable under 35USC 103(a).

3. Regarding claim 60, the number of amplifiers is two.

4. Regarding claim 61, Suzuki et al. shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Suzuki et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

5. Regarding claims 62 and 76, each amplifier stage 241 and 242 comprises differential amplifier.

6. Regarding claim 63, logic circuitry includes said transistor in each amplifier stage is seen as transistors 253-256 and 268-271 of Suzuki et al.'s figure 5.

7. Regarding claims 64, 77 and 79, each amplifier stage of Suzuki et al. inherently has hysteresis characteristics which varies in response to the clock signal.

8. Regarding claim 78, the limitations recited therein is inherently present in Suzuki et al.

9. Regarding claims 65-67 and 80-81 each amplifier stage is CMOS.

10. Regarding claims 68 and 69, said first transistors are seen as 254 and 256 for the odd stage 241, 269 and 271 for the even stage 242, said second transistors are seen as 253 and 255 for the odd stage and 268 and 270 for the even stage. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

11. Regarding claims 70 and 82, Suzuki et al. does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Suzuki et al.'s frequency divider.

12. Regarding claim 72, first and second inverters are seen as transistors 243-244, 248, 249; 257, 258, 262, 263.

13. Regarding claim 73, N channel transistors are seen as transistors 253-256.

14. Regarding claim 74, Suzuki et al. does not disclose the size of n channel controlling transistors (253-256) is larger than the size of n channel transistors (243 and 248). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the crossed inverters (2430244, 248, 249) at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

15. Claims 71 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USP 4,356,411) in view of Maemura (USP 5,172,400), both prior art of record. Figure 5 of Suzuki et al. reference teaches and suggest all limitations recited in claims 59 and 75, as noted above, but fails to show logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 71 and 83. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of Suzuki et al.'s figure for the flexibility of obtaining a frequency divided output other than power of two.

16. Claims 59-73 and 75-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rollins et al. (USP 5,036,217), newly cited prior art. Figure 3B of Rollins et al. shows a frequency divider circuit (600) comprising a first signal means (not shown) to generate a first periodic signal (CLOCK) to be frequency divided by the frequency divider (600), said frequency divider comprises an input terminal for receiving the first periodic signal, an even number of amplifier stages (two amplifier stages 601 and 619) connected in series, with an output of a last amplifier stage (601) connected to input of a first amplifier stage (619) and each amplifier each having an associated propagation delay and a transistor (618, 620) coupled between a supply terminal Vdd and a reference terminal ground for modulating delay through the associated amplifier, wherein the first periodic signal (CLOCK) applied to the first input terminal to a control electrode of the transistor 620 of the odd amplifier stage (619), an even amplifier (601) is

activated in anti-phase of the first periodic signal (CLOCK/), the propagation delay through the associated odd and even amplifier stages (601-619) about half the period of the first periodic signal so that when the propagation delay through the even amplifier stage (601) decreases, the propagation delay through the odd amplifier stage increases, and an output terminal (QO, QO') for outputting a generated frequency divided signal.

The differences seen between Rollins et al. and the present invention are: (1) Rollins et al. uses a single periodic signal (CLOCK) for both even and odd amplifiers instead of the periodic signal and its complementary for even and odd amplifiers stage, respectively, (2) Rollins et al.'s periodic signal is a square wave instead of an analogue periodic signal as called for in claims 59, 75 and 84. Although Rollins et al. uses a single clock, one skilled in the art would have recognize that the even and odd amplifiers (601 and 619) are responsive to positive edges and negative edges, respectively. That is, the even and odd amplifiers (601, 619) operate on complementary phases of the clock signal. One skilled in the art would have been recognized that the N-channel transistor 618 receiving the CLOCK signal is functionally equivalent to P channel transistor receiving the opposite phase of the clock signal (CLOCK). Therefore, it would have been obvious to person skilled in the art at the time of the invention was made to replace the N channel transistor 618 coupled to the clock signal (CLOCK) with P channel transistor coupled to an inverter for receiving a complementary of the clock signal because the substitution is equivalent and will not alter the operation of the frequency divider.

Regarding the input signals being analog periodic signals over square wave signals, one skilled in the art would have recognized that Rollins et al. would perform substantially the same frequency dividing function for both square wave and analog signals. Since, the field effect

transistors are voltage control device, with the analog signal, the field effect transistors will be fully opened or fully closed but to act as variable resistances (see Schilling et al., pages 141 and 147-149). Therefore, outside of non-obvious results, the obvious of using analog signals as input signals instead of square wave to vary the resistance of field effect transistors in a frequency divider will not be patentable under 35USC 103(a).

17. Regarding claim 60, the number of amplifiers is two.

18. Regarding claim 61, Rollins et al. shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Suzuki et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

19. Regarding claims 62 and 76, each amplifier stage 601 and 619 comprises differential amplifier.

20. Regarding claim 63, logic circuitry includes said transistors 606, 608, 610, 612, 614, 166 Rollins et al.'s figure 3B.

21. Regarding claims 64, 77 and 79, each amplifier stage of Rollins. inherently has hysteresis characteristics which varies in response to the clock signal.

22. Regarding claim 78, the limitations recited therein is inherently present in Rollins et al.

23. Regarding claims 65-67 and 80-81 each amplifier stage is CMOS.

24. Regarding claims 68 and 69, said first transistor is seen as 619 for the odd stage 601 and 619, the replaced transistor of transistor 618 for the even stage 601, said second transistors are seen as 622 and 624 for the odd stage and 606 and 616 for the even stage. Said first and second transistors are coupled in series between the supply terminal and the reference terminal.

25. Regarding claims 70 and 82, Rollins et al. does not specifically indicate the periodic signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Rollins et al.'s frequency divider.

26. Regarding claims 71 and 83, the logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two are seen logic gates 502 and 504 shown in figure 3A of Rollins et al.

27. Regarding claim 72, first and second inverters are seen as transistors 626, 628; 602, 604.

28. Regarding claim 73, N channel transistors are seen as transistors 608, 612, 610, 616.

***Conclusion***

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-308-4809. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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September 28, 2002